

Please amend the claims as follows (this listing replaces all other listings):

1. (currently amended) A method comprising:
identifying a plurality of memory resources for pushing data to and pulling data from a
processing agent;
~~arbitrating use of a push bus by using a push bus arbiter; and~~
using a push bus arbiter to arbitrate use of a push bus by the memory resources;
pushing the data from the memory resources to the processing agent through the push
bus, the memory resources obtaining access to the push bus based on arbitration by the push bus
arbiter;
using a pull bus arbiter to arbitrate use of a pull bus by the memory resources; and
pulling the data from the processing agent and transferring to the memory resources
through the pull bus, the memory resources obtaining access to the pull bus based on arbitration
by the pull bus arbiter.
2. (previously presented) The method of claim 1 further comprising:
establishing a plurality of contexts on the programming agent and maintaining program
counters and context relative registers.
3. (original) The method of claim 2 wherein the programming agent executes a
context and issues a read command to a memory controller in a read phase.
4. (previously presented) The method of claim 3 wherein the memory controller
processes the read command to be sent to one of the memory resources.
5. (original) The method of claim 4 wherein the context is swapped out if the read
data is required to continue the execution of the context.

6. (original) The method of claim 5 wherein after the memory controller has completed the processing of the read command, the memory controller pushes the data to an input transfer register of the programming agent.

7. (original) The method of claim 6 wherein after the data has been pushed, the programming agent reads the data in the input transfer register and the programming agent continues the execution of the context.

8-12. (cancelled)

13. (currently amended) A system comprising:
a plurality of memory resources, each memory resource being associated with a memory controller;

a processing agent to access the memory resources;
a push bus to push data from the memory resources to the processing ~~agent; agent;~~ and
a push bus arbiter to arbitrate use of the push bus by the memory resources, the memory resources obtaining access to the push bus based on arbitration by the push bus arbiter;

a pull bus to receive data from the processing agent and to transfer the data to the memory resources; and

a pull bus arbiter to arbitrate use of the pull bus by the memory resources, the memory resources obtaining access to the pull bus based on arbitration by the pull bus arbiter.

14. (previously presented) The system of claim 13 wherein one of the memory resources transfers data to the processing agent unidirectionally during a read phase.

15. (cancelled)

16. (original) The system of claim 13 further comprising a plurality of program counters and a plurality of context relative registers.

17. (original) The system of claim 16 in which the context relative registers are selected from a group comprising of general purpose registers, inter-programming agent registers, static random access memory (SRAM) input transfer registers, dynamic random access memory (DRAM) input transfer registers, SRAM output transfer registers, DRAM output transfer registers, and local memory registers.

18. (original) The system of claim 17 in which the programming agent is to execute a context and issue a read command to a memory controller.

19. (original) The system of claim 18 in which the memory controller is to process the read command to be sent to the memory resource.

20. (original) The system of claim 19 in which the programming agent is to swap the context out if the read command is required to continue to execution of the context.

21. (previously presented) The method system of claim 20 in which after the read command is processed, the memory controller is to push the data to an input transfer register of the programming agent and the programming agent is to read the data in the input transfer register and to continue the execution of the context.

22-25. (cancelled)

26. (currently amended) A machine-accessible medium, which when accessed results in a machine performing operations comprising:

identifying a plurality of memory resources for pushing data to and pulling data from a processing agent, each memory resource being associated with a memory controller;
~~arbitrating use of a push bus by using a push bus arbiter; and~~
using a push bus arbiter to arbitrate use of a push bus by the memory resources;
pushing the data from the memory resources to the processing agent through the push bus, the memory resources obtaining access to the push bus based on arbitration by the push bus arbiter;
using a pull bus arbiter to arbitrate use of a pull bus by the memory resources; and
pulling data from the processing agents and transferring the data to the memory resources through the pull bus, the memory resources obtaining access to the pull bus based on arbitration by the pull bus arbiter.

27. (previously presented) The machine-accessible medium of claim 26, which when accessed further results in the machine performing operations comprising establishing a plurality of contexts on the programming agent and maintaining program counters and context relative registers.

28. (original) The computer program product of claim 26 wherein the programming agent in a read phase executes a context and issues a read command to a memory controller.

29. (original) The computer program product of claim 26 wherein the memory controller processes the read command to be sent to the memory resource and the context is swapped out if the read command is required to continue the execution of the context.

30. (cancelled)

31. (currently amended) The method of ~~claim 30~~claim 1 wherein the programming agent executes a context and loads the data into an output transfer register of the programming agent in a write phase.

32. (previously presented) The method of claim 31 wherein the programming agent issues a write command to a memory controller and the output transfer register is set to a read-only state.

33. (previously presented) The method of claim 32 wherein the context is swapped out if the write command is required to continue the execution of the context.

34. (previously presented) The method of claim 33 wherein the memory controller pushes the data from the output transfer register and the memory controller sends a signal to the programming agent to unlock the output transfer register.

35. (previously presented) The method of claim 34 wherein if the context has been swapped out after the output transfer register has been unlocked, the context is swapped back in and the programming agent continues the execution of the context.

36. (cancelled)

37. (currently amended) The system of ~~claim 36~~claim 13 wherein the processing agent transfers data to one of the memory resources unidirectionally during a write phase.

38. (previously presented) The system of claim 37 in which the programming agent is to execute a context and load the data into an output transfer register of the programming agent.

39. (previously presented) The system of claim 38 in which the programming agent is to issue a write command to a memory controller and in which the output transfer register is set to a read-only state.

40. (previously presented) The system of claim 39 in which the programming agent is to swap the context out if the write command is required to continue to execution of the context.

41. (previously presented) The system of claim 40 in which the memory controller is to push the data from the output transfer register and to send a signal to the programming agent to unlock the output transfer register.

42. (cancelled)

43. (previously presented) The method of claim 1, wherein the memory resources comprise memory controller channels.

44. (previously presented) The system of claim 13, wherein the memory resources comprise memory controller channels.

45. (previously presented) The machine accessible medium of claim 26, wherein the memory resources comprise memory controller channels.

46. (previously presented) The method of claim 30, wherein the memory resources comprise memory controller channels.

47. (previously presented) The system of claim 36, wherein the memory resources comprise memory controller channels.

48. (previously presented) The machine accessible medium of claim 42, wherein the memory resources comprise memory controller channels.